Release Notes

Keysight MIPI M-PHY Command Line Packet Generator

Version 6.10 – August 2015

- Software Version: 06.10.0000
- FPGA Version: 9064

Overview

The Keysight **C**ommand **L**ine **P**acket **G**enerator (CLPG) acts as a stimulus Host and exercises the M-PHY UniPro link. It also has an embedded analyzer with bidirectional data capture and analysis i.e. captures the data that it transmits as stimulus as well as the data that it receives from DUT. The CLPG tool is available as a licensed software option (U4431A-613) of the Keysight U4431A M-PHY Protocol Analyzer module, which is installed in a Keysight AXIe chassis (M9502A).

This document contains information related to this release that is not covered in the printed and on-line documentation for the Command Line Packet Generator.

Operating System Compatibility

Similar to Keysight Logic and Protocol Analyzer software (Main Application), Keysight U4431A M-PHY Command Line Packet Generator (Add-On package) is also 64-bit application. Therefore it is only supported on 64-bit operating systems.

Hardware Components Prerequisites

- Keysight U4431A M-PHY Module installed in a AXIe chassis (M9502A)
- Keysight U4432A SMA Stimulus Probe
- Keysight MIPI M-PHY Loopback Board

Supporting Documentation

- Command Line Packet Generator User Guide (part of CLPG Add-On package)
- Command Line Packet Generator TCL function Help (part of CLPG Add-On package)
- Logic and Protocol Analyzer Readme (part of Main application)
- Logic and Protocol Analyzer Online Help (part of Main application)

Software Installation Notes

Install the following software components in the specified sequence before starting

- Keysight Logic and Protocol Analyzer (LPA) version 06.10.0000 or higher

KEYSIGHT TECHNOLOGIES

- Active TCL 8.5 (32 bit)
- TCOM package (TCL COM Interface)
- Keysight Command Line Packet Generator (CLPG) Add-On Package

Licensing

- U4431A-613 (Command-line packet generator) license option of the Keysight U4431A M-PHY Protocol Analyzer module is required to use this software build

Usage Notes / Known Limitations

1. Minimum lock time required at HS-G2 and HS-G3 speed is 128 symbol time. So DUT should be configured to transmit burst with128 Sync symbols at least.
2. Selection between rate series A and B should be done manually through GUI for embedded analyzer and TCL function for CLPG.
3. Physical to logical lane mapping should be manually configured before link start up sequence.
4. M-TX and M-RX works with same link width, mode and gear.
5. PWM data rate is fixed for each gear during transmission.
6. Single Traffic class TC0 is supported.
7. Number of CPort supported is one.
8. Prepare length, Sync length and Idle time (to enter Sleep/Stall) are fixed during transmission.
9. CLPG doesn't transmit pre-empted frames.
10. The maximum size of Receiver buffer is 16*272 bytes. If the message is 272 bytes or less, it will consume 1*272 of 16*272 bytes buffer. If the message is greater than or equal to 3*272 bytes, it will consume 3*272 of 16*272 bytes buffer. Any data that is received beyond 16*272 bytes buffer will not be buffered.
11. The maximum size of Transmit buffer is 16*272 bytes. If the message is 272 bytes or less, it will consume 1*272 of 16*272 bytes buffer. If the message is greater than or equal to 3*272 bytes, it will consume 3*272 of 16*272 bytes buffer.
12. Embedded analyzer captures protocol frames from both directions A (DUT) and B (CLPG). It can also capture raw data of direction A (DUT).
13. Trigger can be configured on frames from direction A (DUT) only.
14. Embedded analyzer tracks link configuration based on direction A (DUT).
15. Correlation between embedded analyzer and second blade (if plugged-in) is not supported.

Software Revision History

None